

## CLAIMS

What is claimed is:

- 1 1. An integrated circuit (IC) package substrate comprising a plurality of  
2 conductors within an IC mounting region, each conductor to be electrically coupled  
3 to a respective terminal of an IC, and at least one capacitor within the IC mounting  
4 region.
- 1 2. The IC package substrate recited in claim 1, wherein the at least one  
2 capacitor is electrically coupled to at least one conductor.
- 1 3. The IC package substrate recited in claim 2, wherein the at least one  
2 capacitor is mounted atop the at least one conductor.
- 1 4. The IC package substrate recited in claim 3, wherein the at least one  
2 capacitor is a capacitor array comprising two surfaces, each having a plurality of  
3 terminals of first and second polarity types.
- 1 5. The IC package substrate recited in claim 4, wherein the plurality of  
2 terminals of the capacitor array are disposed over substantially the entire surfaces.
- 1 6. The IC package substrate recited in claim 2, wherein the at least one  
2 capacitor is mounted beside the at least one conductor.
- 1 7. The IC package substrate recited in claim 1, wherein the conductors include  
2 at least one conductive bar having a height and a width, the height exceeding the  
3 width, and wherein the at least one capacitor is mounted beside and in electrical  
4 contact with the at least one conductive bar.
- 1 8. The IC package substrate recited in claim 1, wherein the plurality of  
2 conductors are substantially parallel to one another.

1 9. The IC package substrate recited in claim 8, wherein the at least one  
2 capacitor is non-orthogonally mounted atop the at least one conductor.

1 10. The IC package substrate recited in claim 1 and comprising a plurality of  
2 capacitors distributed substantially throughout the IC mounting region, each  
3 capacitor being in electrical contact with at least one of the conductors.

1 11. The IC package substrate recited in claim 10, wherein the plurality of  
2 capacitors comprises a plurality of sets of capacitors, each set comprising one or  
3 more capacitors aligned substantially end-to-end.

1 12. The IC package substrate recited in claim 1, wherein the conductors include  
2 pads.

1 13. An integrated circuit (IC) comprising:  
2 a plurality of conductive bars on a surface of the IC, each conductive bar to  
3 be electrically coupled to a respective terminal of an IC package substrate; and  
4 at least one capacitor having terminals coupled to at least two of the  
5 conductive bars.

1 14. The IC recited in claim 13, wherein the conductive bars have a height and a  
2 width, the height exceeding the width.

1 15. The IC recited in claim 14, wherein the at least one capacitor is mounted  
2 beside and in electrical contact with the at least two conductive bars.

1 16. An integrated circuit (IC) package comprising:  
2 a substrate having a plurality of conductors within an IC mounting region;

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3 at least one capacitor within the IC mounting region and electrically coupled  
4 to at least one of the conductors; and  
5 an IC electrically coupled to the plurality of conductors.

1 17. The IC package recited in claim 16, wherein the at least one capacitor is  
2 electrically coupled to first and second conductors of the plurality of conductors,  
3 and wherein the first conductor is to couple to a first potential, and the second  
4 conductor is to couple to a second potential.

1 18. The IC package recited in claim 16, wherein the at least one capacitor is  
2 mounted atop the at least one conductor.

1 19. The IC package recited in claim 18, wherein the at least one capacitor is  
2 mounted atop two conductors.

1 20. The IC package recited in claim 18, wherein the at least one capacitor is an  
2 capacitor array having two surfaces, each having a plurality of terminals of first and  
3 second polarity types.

1 21. The IC package recited in claim 20, wherein the plurality of terminals are  
2 disposed over substantially the entire surfaces.

1 22. The IC package recited in claim 16, wherein the at least one capacitor is  
2 mounted beside the at least one conductor.

1 23. The IC package recited in claim 16, wherein the at least one capacitor is  
2 mounted between two conductors.

1 24. The IC package recited in claim 16, wherein the at least one capacitor has a  
2 top, a bottom, and a pair of opposing sides, and wherein the at least one capacitor is

3 from the group comprising a capacitor having terminals on its top and bottom, a  
4 capacitor having terminals on its opposing sides, and a capacitor having terminals  
5 on its top, bottom, and opposing sides.

1 25. The IC package recited in claim 16, wherein the conductors include at least  
2 one conductive bar having a height and a width, the height exceeding the width, and  
3 wherein the at least one capacitor is mounted beside and in electrical contact with  
4 the at least one conductive bar.

1 26. The IC package recited in claim 16, wherein the plurality of conductors are  
2 substantially parallel to one another.

1 27. The IC package recited in claim 26, wherein the at least one capacitor is  
2 non-orthogonally mounted atop the at least one conductor.

1 28. The IC package recited in claim 16 and comprising a plurality of capacitors  
2 distributed substantially throughout the IC mounting region, each capacitor being in  
3 electrical contact with at least one of the conductors.

1 29. The IC package recited in claim 28, wherein the plurality of capacitors  
2 comprises a plurality of sets of capacitors, each set comprising one or more  
3 capacitors aligned substantially end-to-end.

1 30. The IC package recited in claim 16, wherein the conductors include pads.

1 31. An electronic assembly comprising:  
2 a printed circuit board (PCB); and  
3 an integrated circuit (IC) package coupled to the PCB and including  
4 a substrate having a plurality of conductors within an IC mounting  
5 region;

6 at least one capacitor within the IC mounting region and electrically  
7 coupled to at least one of the conductors; and  
8 an IC electrically coupled to the plurality of conductors.

1 32. The electronic assembly recited in claim 31, wherein the at least one  
2 capacitor is electrically coupled to two of the conductors, one conductor to couple to  
3 a first potential, the other conductor to couple to a second potential.

1 33. The electronic assembly recited in claim 31, wherein the at least one  
2 capacitor is mounted atop the at least one conductor.

1 34. The electronic assembly recited in claim 31, wherein the at least one  
2 capacitor is mounted beside the at least one conductor.

1 35. An electronic system comprising:  
2 a bus coupling components in the electronic system;  
3 a display coupled to the bus;  
4 external memory coupled to the bus; and  
5 a processor coupled to the bus and comprising an electronic assembly  
6 including:  
7 a printed circuit board (PCB); and  
8 an integrated circuit (IC) package coupled to the PCB and including  
9 a substrate having a plurality of conductors within an IC mounting  
10 region;  
11 at least one capacitor within the IC mounting region and electrically  
12 coupled to at least one of the conductors; and  
13 an IC electrically coupled to the plurality of conductors.

1 36. The electronic system recited in claim 35, wherein the at least one capacitor  
2 is mounted atop the at least one conductor.

1 37. The electronic system recited in claim 35, wherein the at least one capacitor  
2 is mounted beside the at least one conductor.

1 \ 38. A method of fabricating an IC package substrate comprising:  
2 arranging a plurality of capacitors on a surface of an integrated circuit (IC)  
3 package substrate within an IC mounting region thereof; and  
4 securing the plurality of capacitors to the surface.

1 39. The method recited in claim 38, wherein the surface comprises a plurality of  
2 conductors, wherein each capacitor comprises terminals of first and second polarity  
3 types, and wherein, in arranging, the plurality of capacitors are disposed such that  
4 terminals of the first polarity type contact a first set of the plurality of conductors,  
5 and terminals of the second polarity type contact a second set of the plurality of  
6 conductors.

1 40. The method recited in claim 38, wherein, in securing, a fill material is  
2 applied to the plurality of capacitors and to openings between the capacitors.

1 \ 41. A method comprising:  
2 forming at least one capacitor assembly, the at least one capacitor assembly  
3 having at least one capacitor electrically coupled to a conductor; and  
4 mounting the at least one capacitor assembly to a surface of an integrated  
5 circuit (IC) package substrate within an IC mounting region thereof.

1 42. The method recited in claim 41, wherein the conductor comprises a  
2 conductive bar having a height and a width, the height exceeding the width.

1 43. The method recited in claim 41 and further comprising:  
2 applying a fill material to the at least one capacitor assembly.

1 44. A method comprising:  
2 arranging a plurality of capacitors within an IC mounting region on a surface  
3 of an integrated circuit (IC) package substrate; and  
4 mounting an IC on the mounting region.

1 45. The method recited in claim 44, wherein, in arranging, the plurality of  
2 capacitors are coupled to electrical conductors within the IC mounting region.

1 46. The method recited in claim 45, wherein the IC has a plurality of terminals,  
2 and wherein, in arranging, at least one capacitor of the plurality of capacitors is  
3 coupled between a respective IC terminal and a respective electrical conductor  
4 within the IC mounting region.

1 47. The method recited in claim 44, wherein, in arranging, the plurality of  
2 capacitors are coupled to electrical conductors within the IC mounting region, the  
3 electrical conductors including a plurality of conductive bars each having a height  
4 and a width, the height exceeding the width.

1 48. The method recited in claim 47, wherein, in arranging, at least one capacitor  
2 of the plurality of capacitors is coupled between adjacent ones of the plurality of  
3 conductive bars.

1 49. The method recited in claim 44, wherein, in mounting, the IC is electrically  
2 coupled to the plurality of capacitors.

1 50. A method comprising:  
2 placing a capacitor array within an IC mounting region on a surface of an  
3 integrated circuit (IC) package substrate; and  
4 mounting an IC on the mounting region.

1 51. The method recited in claim 50, wherein the capacitor array has a plurality  
2 of terminals, and wherein, in placing, the plurality of terminals of the capacitor array  
3 are coupled to respective conductors within the IC mounting region.

1 52. The method recited in claim 51, wherein the IC has a plurality of terminals,  
2 and wherein, in mounting, the plurality of terminals of the IC are coupled to  
3 respective ones of the plurality of terminals of the capacitor array.

1 \ 53. A method comprising:  
2 forming at least one capacitor assembly, the at least one capacitor assembly  
3 having at least one capacitor electrically coupled to a conductor; and  
4 mounting the at least one capacitor assembly to a surface of an integrated  
5 circuit (IC).

1 54. The method recited in claim 53, wherein the conductor comprises a  
2 conductive bar having a height and a width, the height exceeding the width.

1 55. The method recited in claim 53 and further comprising:  
2 applying a fill material to the at least one capacitor assembly.

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1 \ 56. A method comprising:  
2 arranging a plurality of capacitors on a surface of an integrated circuit (IC);  
3 and  
4 mounting the IC on a mounting region of an IC package substrate.

1 57. The method recited in claim 56, wherein, in arranging, the plurality of  
2 capacitors are coupled to electrical conductors on the IC surface.

1 58. The method recited in claim 57, wherein the IC package substrate has a  
2 plurality of terminals, and wherein, in arranging, at least one capacitor of the  
3 plurality of capacitors is coupled between a respective IC package substrate terminal  
4 and a respective electrical conductor on the IC surface.

1 59. The method recited in claim 56, wherein, in arranging, the plurality of  
2 capacitors are coupled to electrical conductors on the IC surface, the electrical  
3 conductors including a plurality of conductive bars each having a height and a  
4 width, the height exceeding the width.

1 60. The method recited in claim 59, wherein, in arranging, at least one capacitor  
2 of the plurality of capacitors is coupled between adjacent ones of the plurality of  
3 conductive bars.

1 61. The method recited in claim 56, wherein, in mounting, the IC package  
2 substrate is electrically coupled to the plurality of capacitors.

1 62. A method comprising:  
2 forming a first set of conductive bars on a surface of an integrated circuit  
3 (IC) package substrate;  
4 forming a second set of conductive bars on a surface of an IC;  
5 affixing at least one capacitor to at least two conductive bars from the group  
6 comprising the first and second sets of conductive bars; and  
7 mounting the IC on an IC mounting region of the IC package substrate.

1 63. The method recited in claim 62, wherein, in forming, the conductive bars  
2 have a height and a width, the height exceeding the width, and wherein the height of  
3 the first set of conductive bars is substantially identical to the height of the second  
4 set of conductive bars.

